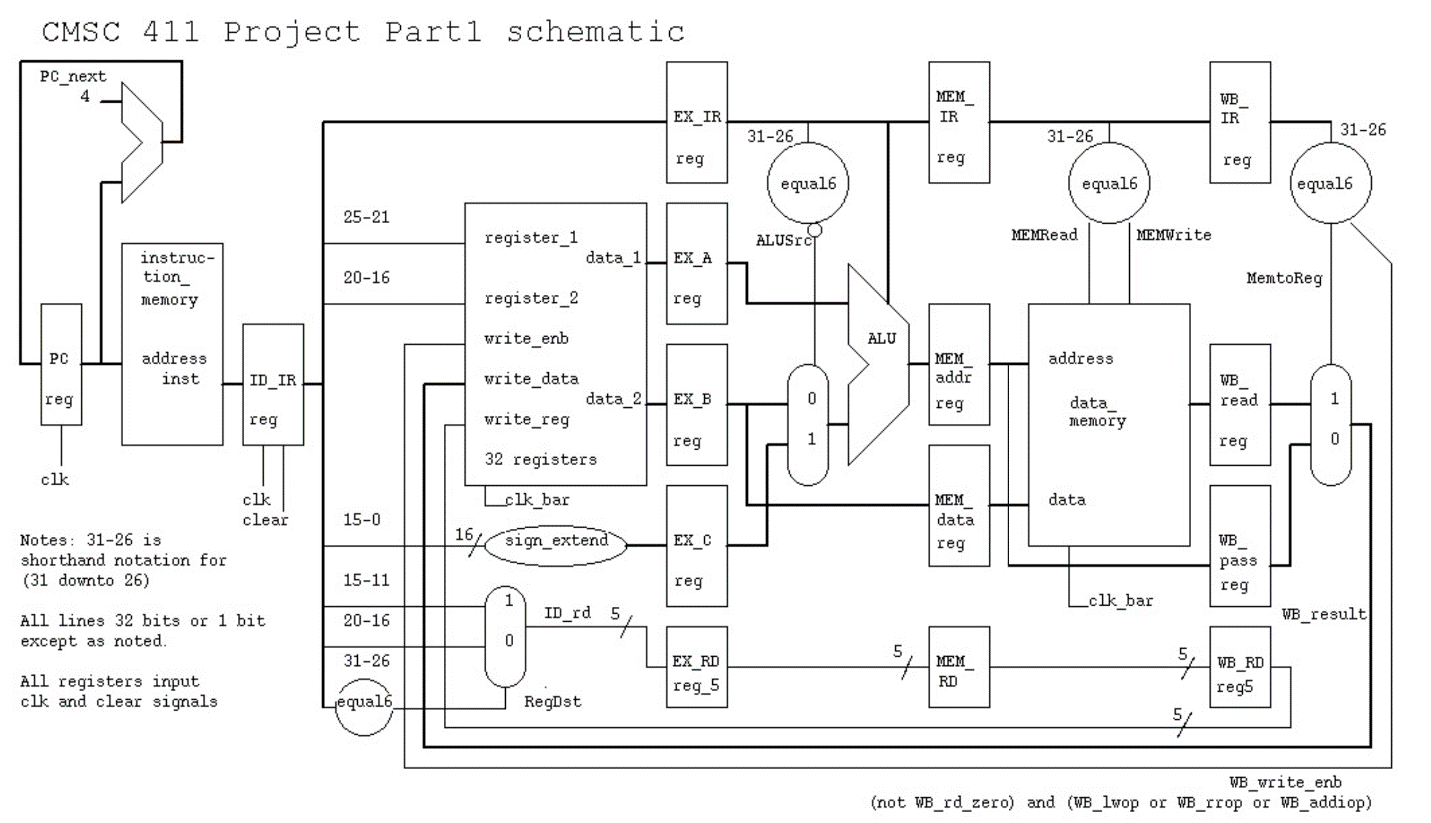
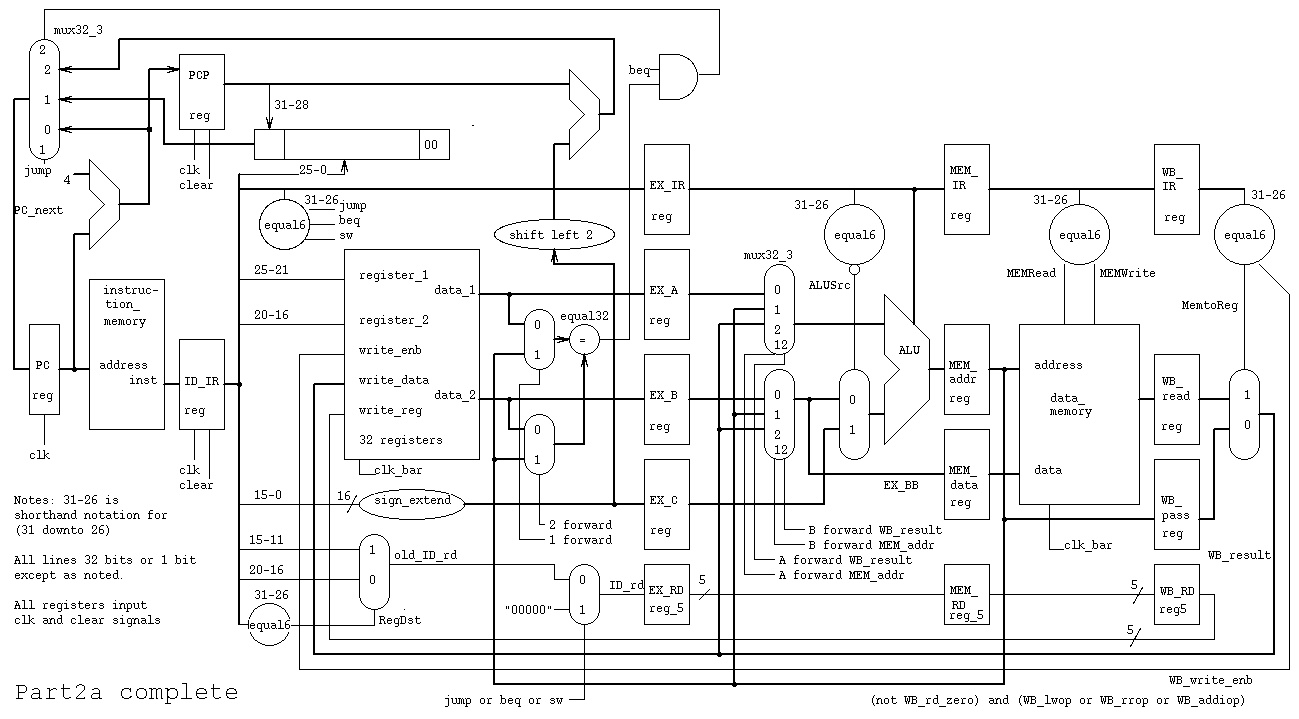
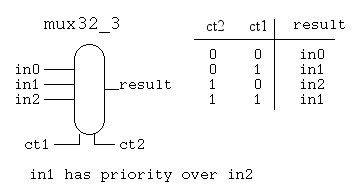
411 images for each part. **NOTE: these are the images from spring 2020 but the code corresponds to the images used in 2019. There may be some discrepancies.**

Part 1



Part 2a





library IEEE;

use IEEE.std\_logic\_1164.all;

entity mux32\_3 is

port(in0 : in std\_logic\_vector (31 downto 0);

in1 : in std\_logic\_vector (31 downto 0);

in2 : in std\_logic\_vector (31 downto 0);

ct1 : in std\_logic; -- pass in1(has priority)

ct2 : in std\_logic; -- pass in2

result : out std\_logic\_vector (31 downto 0));

end entity mux32\_3;

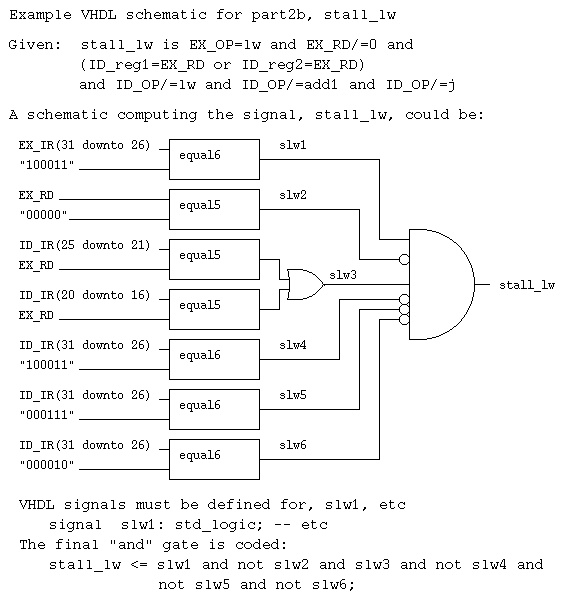
architecture behavior of mux32\_3 is

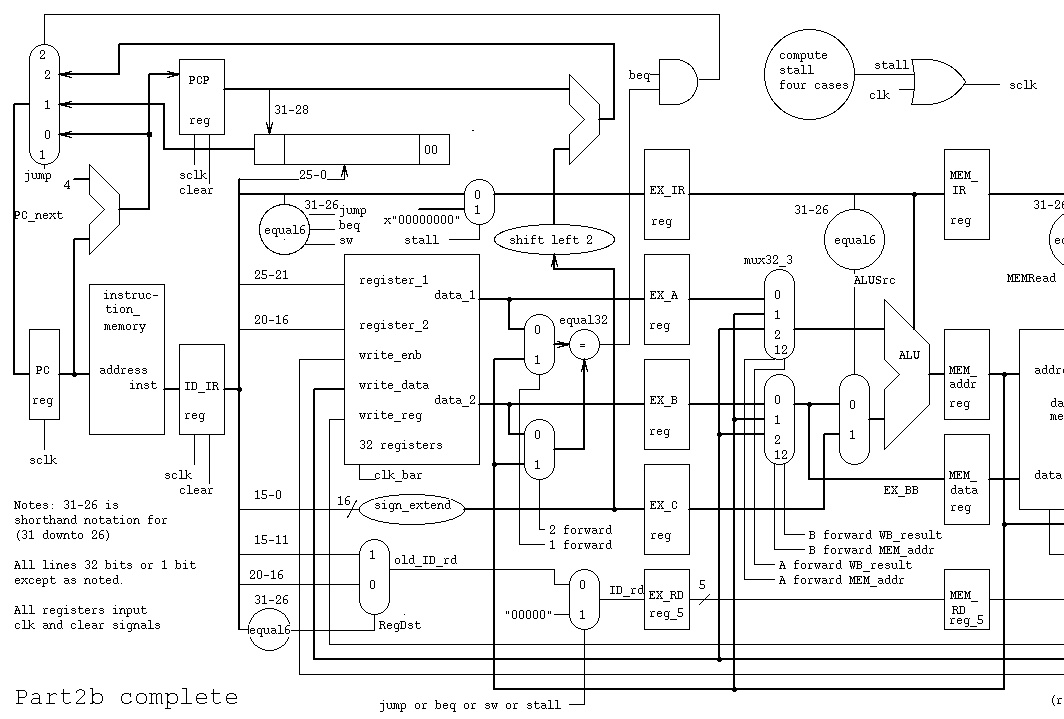
begin -- behavior -- no process needed with concurrent statements

result <= in1 when ct1='1' else in2 when ct2='1' else in0 after 50 ps;

end architecture behavior; -- of mux32\_3

Part 2b





Part 3a

